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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/625,693	07/24/2003	Mayur Joshi	M4065.0929/P929	9940

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DICKSTEIN SHAPIRO MORIN & OSHINSKY LLP
2101 L STREET NW
WASHINGTON, DC 20037-1526

EXAMINER	
WILLIAMS, HOWARD L	
ART UNIT	**PAPER NUMBER**
2819	

DATE MAILED: 07/12/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/625,693	JOSHI, MAYUR	
	Examiner	Art Unit	
	Howard L. Williams	2819	

-- The MAILING DATE of this communication appears on the cover sheet with the c rrespondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-58* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *6-13, 24-31, 35-37, 45-48, 52, 54 and 58* is/are allowed.

6)☐ Claim(s) *1-5, 14, 16- 23, 32-34, 38, 40-42, 44, 49-51, 53 and 55-57* is/are rejected.

7)☐ Claim(s) *15, 39 and 43* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10) ☒ The drawing(s) filed on *06 November 2003* is/are: a) ☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *093003*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

The number of claims presented is unreasonably excessive for the subject matter.

The examiner acknowledges receipt of an information disclosure statement on 30 September 2003. An initialed copy of the citation form should accompany this letter.

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> *(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.*

Claims 1-5, 38, 40-42 and 44 are rejected under 35 U.S.C. 103(a) as unpatentable over Mihara (US 5418923 A) in view of Foss et al. (US 6580652 B2).

Mihara discloses (fig. 1) a priority encoder (7) and ROM encoder (9). The ROM encoder (9) receives M input lines (T1-T8), only one of which is active at time, and provides binary codes on the N output lines (F0-F2). Notably $M = 2^N$. Reviewing the connections shown for the encoder (9) the adjacent output lines for k= 0 to (*sic*) (M/2 – 1) – it is presumed that the expression ((M/2) – 1) is what was meant— the 2kth and (2k+1)th codes are complementary. Mihara does not fully illustrate the dotted interconnections between the input lines (horizontal T1-T8) and the vertical lines leading to the OR gates. Mihara also does not disclose the use of domino logic (dynamic OR) to effect the encoding function.

Foss et al. discloses a ROM encoder using domino logic as evidenced by the clock precharging in figure 3 (col. 8, lines 1-4) and shows the switching transistors, specifically NMOS. It would have been obvious to one of skill in the art to use domino logic to provide the faster output available from the pre-charging and compact encoder structure available with domino logic. Although, Mihara shows M = 8 and N = 3, it is

considered well within one of skill in the art to recognize that these numbers may change.

Considering claim 14, the dotted connections representing switching transistors in Mihara the switching elements have at most one neighboring switching element controlling the same output line. The input lines also still have at most one asserted bit and that one neighbor of an output line provides complementary codes.

Considering claims 40-42 Foss as before shows the transistors connected to the input lines to achieve the connection represented by the dotted lines in Mihara and use dynamic OR logic.

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> *A person shall be entitled to a patent unless –*
> *(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.*

Claims 18-23 and 32-34 are rejected under 35 U.S.C. 102(b) as anticipated by Mihara (US 5418923 A). These claims drawn to the encoding function verbosely recite no more than input lines, output lines and complementary output codes for the respective one neighboring line. This has already been addressed in the discussion of Mihara above in connection with obviousness rejection of claims 1-5 minus the switching elements.

Claims 38 and 44 are rejected under 35 U.S.C. 103(a) as being unpatentable over Mihara (US 5418923 A). Mihara does not disclose the substrate but shows (figs. 1 and 3), the CAM (associative memory), priority encoder circuitry and address encoder circuitry (7, 8, 9; fig. 1). It would have been obvious to include a substrate for an IC because each of the items above are well known to be commonly produced in IC form on a substrate with a surface.

Claims 49-51, 53 and 55-57 are rejected under 35 U.S.C. 103(a) as unpatentable over Mihara (US 5418923 A) in view of Foss et al. (US 6580652 B2) and Nataraj et al. (US 6757779 B1). These claims in addition to various encoder limitations previously addressed (complementary outputs, one neighbor, nor-ordinal code) recite a processor or router and processor with a CAM. Nataraj et al. discloses router and processor as used with CAM (fig. 75 and columns 1 and 2). It would have been obvious to use CAM circuitry such as disclosed by Mihara with its encoding circuitry to provide the reliable router interface and rule implementation disclosed by Nataraj et al. for the flexible look-up and rule programming provided by CAMs.

Claims 15, 39 and 43 objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Claims 24-31, 35-37, 45-48, 52, 54 and 58 are allowed.

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. US 6028452 A to Benschneider discloses a priority encoder and illustrate substrate implementation of the transistor but refers to only tight pitch and US 5557275 A to van Valburg et al. discloses another binary encoding ROM.

Any inquiry concerning this communication should be directed to Howard L. Williams at telephone number 571.272.1815. The Patent and Trademark Office has a new central facsimile number for application specific correspondence intended for entry, it is 703-872-9306.

7/8/04
Voice 571.272.1815

Howard L. Williams
Primary Examiner
Art Unit 2819